A 3D stacked nanowire technology. Applications in advanced CMOS and beyond

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ABSTRACT

In this paper we will present CMOS nanowire matrices technologies recently developed by using a top down approach. Some electrical and mechanics properties as well as possible interests of the obtained nanowire structures will be discussed both for sub-22nm advanced CMOS devices and for ultimate co-integration of novel functionalities. Some specific needs for characterization and metrology will be discussed, in particular in line 3D critical dimensions measurements and out of line structural characterisation. For CMOS scaling, Silicon-On-Insulator (SOI) nanowires or innovative Silicon-On-Nothing (SON) based 3D stacked technologies are proposed with common or independent gates. Ultra-low static consumption (I_{OFF}<50pA/µm) as well as high driving current (up to I_{ON}=6.5mA/µm) are achieved thanks to 3D stacked Gate-All-Around (GAA) nanowire channels. The top-down nanowire techniques also open up new opportunities for hybridizing CMOS with novel functionalities such as 3D memories, nano-oscillators and bio nano-sensors. In particular, for ultra low mass sensing applications, a few molecule aggregates (i.e a few 10^{-21} g to 10^{-24} g) could be measured with enhanced surface capture through 3D stacking.

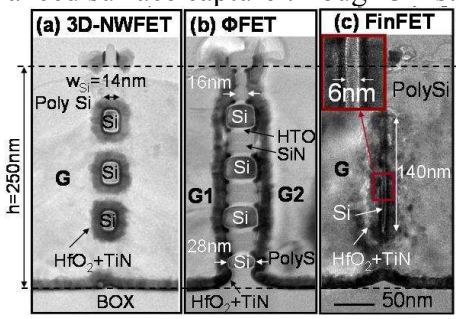

FIGURE 1. Left. Cross-sectional TEM pictures of (a) 3D-NWFET: 15nm-diameter stacked nanowires are obtained (b) ΦFET: Spacers are introduced to obtain stacked nanowires with independent gate operation (c) FinFET: a very high aspect ratio (AR) is obtained (6nm×140nm, AR=23)

REFERENCES

1. T. Ernst et al., IEDM Tech. Dig., pp. 997, 2006.
3. C. Dupré et al. IEDM Techn. Dig., 2008
2. T.Ernst et al. IEDM Techn. Dig., 2008
4. A. Hubert et al., ECS Trans., 13(1), 195-199, 2008.
5. L. Duraffourg et. Al, APL 92, 174106, 2008.
6. R. He and P. Yang, Nature Nanotechnology, vol. 1, p. 42-46 2006

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